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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,127	12/22/2000	Young-Hee Mun	12597-P66182US0	7925

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JACOBSON HOLMAN PLLC
400 SEVENTH STREET N.W.
SUITE 600
WASHINGTON, DC 20004

EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	9

DATE MAILED: 11/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,127	MUN, YOUNG-HEE	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this c mmunication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamatsuka et al (WO 00/12786), where US 6,413,310 is used as an accurate translation, but a translation of WO 00/12786 will be provided upon request.

Tamatsuka et al discloses slicing a silicon single crystal into a wafer, subjecting the wafer to heat treatment at a temperature of 1100-1300°C for 1 minute or more in a non-oxidative atmosphere of argon, nitrogen or a mixed gas of argon or nitrogen which does not have hydrogen at the lower explosion limit or more (col 13, ln 1-40 of '310) and successively subjecting the wafer to a heat treatment at a temperature of 700-1300°C for 1 minute or more, where grown in defects in the wafer surface layer can be eliminated or reduced within a short period of time (col 2, ln 1-67 of '310).

Tamatsuka et al does not disclose a heat treatment on the wafer at a temperature equal to or higher than 1200°C or a rapid thermal annealing at a temperature equal to or lower than 800°C. Overlapping ranges are held to be obvious. (MPEP 2144.05).

Also Tamatsuka et al does not explicitly teach a rapid thermal annealing. It is inherent to Tamatsuka et al's second heat treatment to be a rapid thermal annealing because the duration of the annealing is for 1 minute, which is similar to applicant's annealing duration.

If the heat treatment of Tamatsuka et al is not a rapid thermal annealing, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Tamatsuka et al by using a rapid thermal annealing to reduce processing time.

Referring to claim 2, Tamatsuka et al teaches annealing for greater than 1 minute. Overlapping ranges are held to be obvious (MPEP 2144.05).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamatsuka et al (WO 00/12786), where US 6,413,310 is used as an accurate translation, but a translation of WO 00/12786 will be provided upon request, in view of Limb et al (US 5,352,615).

Nagasawa et al discloses all of the limitations of claim 4, as discussed previously in claims 1-3, except flow the inert gas, first mixed gas and second mixed gas ranges from 2 to 50 slm.

In a method of denuding a semiconductor substrate, Limb et al teaches denuding by heating a substrate to a temperature of 1000-1250°C with a total gas flow rate during processing of 5-20 slpm and an inert gas **313** flows into the furnace, wherein oxygen partial pressure is low to remove native oxide (col 3, ln 20-45 and col 2, ln 55-67).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Tamatsuka et al by using the gas flow rate taught by Limb et al because to form a denuded substrate.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa et al (US 4,376,657) in view of Jastrzebski et al (US 4,429,047) along with Falster (US 5,882,989).

Tamatsuka et al discloses all of the limitations of claim 5, as discussed previously in claims 1-4, except the first heat treatment is from 5 to 100°C/min and a rate of cooling after the first heat treatment is from 5 to 100°C/min.

In a method for determining the oxygen content of a semiconductor material, Jastrzebski et al teaches silicon wafers were heated to 1300°C for one hour and cooled at a rate of 30°C/min (col 6, ln 15-50 and Fig 7). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Tamatsuka et al with Jastrzebski et al cooling rate because a minimum cooling rate is needed to maintain the oxygen in interstitial potions in the lattice.

In a method of preparing silicon wafers having a controlled distribution of oxygen precipitate nucleation centers, Falster annealing out nucleation centers at a temperature of at least 1000°C, where the heating rate is at least 10°C per minute (col 4, ln 10-26). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Tamatsuka et al with Falster's heating rate to prevent some or all of the oxygen precipitate nucleation centers from stabilizing by the heat treatment (col 4, ln 27-35).

5. Claims 17-19, as interpreted by the examiner, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264) in view of Matsushita (4,193,783).

Iida et al discloses a method of growing a silicon single crystal, note entire reference, where the temperature gradient in an in-crystal descending temperature zone in the vicinity of the

solid-liquid interface was set as the gradient at the edge of the ingot was 45.0 (°C/cm) and the gradient at the center of the ingot was 42.0 (°C/cm) and pulling rate was increased resulting in an Oxidation-induced stacking fault (OSF) to appear at a circumferential part with a center region consisting of a vacancy rich region. Iida et al also teaches wafers were sliced from the ingot and measured for defect density (col 14, ln 20-67; col 15, ln 1-15 and FIG 10A).

Iida et al does not disclose extending an area in which delta (Oi) is greatly increased as compared to that of other areas, wherein the delta (Oi) is a difference between an initial oxygen concentration and oxygen concentration after heat treatment with a predetermined thermal history.

In a method of treating a silicon single crystal ingot, note entire reference, Matsushita teaches an ingot **2** is annealed with heat applied for at least 15 hours at a temperature of 1000°C in an atmosphere of nitrogen, this reads on applicant's heat treatment with a predetermined thermal history (col 2, 28-67). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida et al with Matsushita because lattice defects do not arise in the silicon wafer during subsequent manufacturing and impurities are substantially removed after the heat treatment (col 3, ln 15-30). It is inherent the invention taught by the combination of Iida et al and Matsushita to extend an area in which delta is greatly increased as compared to that of other area because the combination of Iida et al and Matsushita teaches a similar heat treatment as applicant and similar method of making a silicon ingot with a OSF ring at the circumferential part.

Referring to claim 18, the combination of Iida et al and Matsushita teaches a heat treatment of at least 15 hours at a temperature of 1000°C in an atmosphere of nitrogen. The

combination of Iida et al and Matsushita does not teach a heat treatment at 1000°C for 64 hours in N_2. Overlapping ranges are held to be obvious (MPEP 2144.05).

Referring to claim 19, it is inherent to the combination of Iida et al and Matsushita to have an area in which delta is greatly increased is formed to occupy 20 to 90% of a diameter of the ingot because the combination of Iida et al and Matsushita teaches a similar heat treatment as applicant and similar method of making a silicon ingot with a OSF ring at the circumferential part with a vacancy region occupying 20-90% of a diameter of an ingot (Fig 10a).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264) in view of Matsushita (4,193,783) as applied to claims 17-19 above, and further in view of Nagasawa et al (US 4,376,657).

The combination of Iida et al and Matsushita teaches moving an oxidation-induced stacking fault (OiSF) ring from the center of a single crystalline growth axis by increasing the rate of pulling and a heat treatment in a N_2 ambience at 1000°C for 64 hours, where the first area and second area in which delta is inherently increased because the combination of Iida et al and Matsushita teaches a similar heat treatment and pulling process as applicant and forming wafers by slicing the ingot, as discussed previously in claims 17-19 above.

The combination of Iida et al and Matsushita does not teach carrying out a first heat treatment on a wafer at a temperature equal to or higher than 1200°C and carrying out a second heat treatment on a wafer by rapid thermal annealing at a temperature equal to or lower than 800°C.

Tamatsuka et al discloses slicing a silicon single crystal into a wafer, subjecting the wafer to heat treatment at a temperature of 1100-1300°C for 1 minute or more in a non-oxidative atmosphere of argon, nitrogen or a mixed gas of argon or nitrogen which does not have hydrogen at hydrogen at the lower explosion limit or more (col 13, ln 1-40 of '310) and successively subjecting the wafer to a heat treatment at a temperature of 700-1300°C for 1 minute or more, where grown in defects in the wafer surface layer can be eliminated or reduced within a short period of time (col 2, ln 1-67 of '310). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Iida et al and Matsushita to eliminate or reduce defects in a wafer. Overlapping ranges are held to be obvious (MPEP 2144.05).

The combination of Iida et al, Matsushita and Tamatsuka et al teaches a second heat treatment for a period of 1 min or more. The combination of Iida et al, Matsushita and Tamatsuka et al is silent to the treatment is a rapid thermal annealing. It is inherent to the combination of Iida et al, Matsushita and Tamatsuka et al that the second annealing is a rapid thermal annealing because the combination of Iida et al, Matsushita and Tamatsuka et al teaches a similar annealing period, as applicant. If it is not inherent to the combination of Iida et al, Matsushita and Tamatsuka et al to have a rapid thermal annealing, then it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Iida et al, Matsushita and Tamatsuka et al by employing a rapid thermal annealing to reduce processing time.

Response to Arguments

7. Applicant's arguments with respect to claims 1-7 and 8 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 10/10/2002 have been fully considered but they are not persuasive.

In response to applicant's argument in regard to claim 17, Applicant's argue that claim 17 is directed to a method of forming wafer which include a vacancy rich region. The cited prior art, namely Iida et al, teaches the formation of a vacancy rich region in Fig 10A. Iida et al is directed to forming a N-region as suggested by applicant at a pulling speed of approximately 0.55 mm/min, but Iida et al also teaches forming a vacancy rich region at a pulling speed greater than approximately 0.6 mm/min, where the vacancy region encompasses 20-90% of the diameter of the growing ingot.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., method of forming wafers which include a vacancy rich region) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on 703-308-3868. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS
November 21, 2002

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700